US-PAT-NO: 6323132

DOCUMENT-IDENTIFIER: US 6323132 B1

TITLE: Etching methods for anisotropic platinum profile

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Because the platinum electrode layer 16 easily diffuses or reacts with certain elements (e.g. a poly-Si plug) within the semiconductor substrate 12, the barrier layer 14 is required between the platinum electrode layer 16 and the semiconductor substrate 12. The barrier layer 14 also functions as an **adhesive** for coupling the semiconductor substrate 12 to the **platinum** electrode layer 16. A mask 18 is disposed over the platinum electrode layer 16 and a patterned resist (i.e. a photoresist), generally illustrated as 20, is selectively positioned on the mask layer 18 as best shown in FIG. 1. As best shown in FIG. 1, the patterned resist 20 includes a plurality of resist members 20a, 20b, 20c, and 20d. In another preferred embodiment of the invention as shown in FIG. 2, a protective layer 22 is disposed between the platinum electrode layer 16 and the mask layer 18.

The barrier layer 14 may be any suitable barrier layer which is capable of dually functioning as an **adhesive** and a diffusion barrier to the **platinum** electrode layer 16. The barrier layer 14 may be of any suitable thickness. Preferably, the barrier layer 14 comprises titanium and/or a titanium **alloy**, such as TiN, and possesses a thickness ranging from about 50 Angstroms to about 600 Angstroms, more preferably from about 200 Angstroms to about 400 Angstroms,

most preferably about 300 Angstroms. The barrier layer 14 is preferably
disposed on the semiconductor substrate 12 by the RF magnetron sputtering
method.

US-PAT-NO: 6208400

DOCUMENT-IDENTIFIER: US 6208400 B1

TITLE: Electrode plate having metal electrodes of aluminum or nickel and
copper or silver disposed thereon

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More specifically, the undercoat layer 11a (or 11b) may preferably be a
0.01-0.3 .mu.m thick film of a metal or **alloy** having a good adhesiveness
(**adhesive** properties) to the glass substrate 6a (6b). Examples of such a metal
or alloy include a single metal, such as ~~Ti (titanium)~~, Cr (chromium), Mo
(molybdenum), W (tungsten), Al (aluminum), Ta ~~(tantalum)~~, Ni (nickel); and
~~alloys of these metals~~.

Further, the use of the undercoat layer 11c of Ni--Mo **alloy** exhibiting a high
adhesive property, the low-resistance metal layer 12 of Cu exhibiting a high
electrical conductivity, and the protective layer 13 of Ni exhibiting an
anti-oxidizing property better than Cu bring about various advantageous effects
as described in the preceding embodiments (First to Ninth embodiments).

When a ample substrate using Ni--Mo **alloy** (Mo:8.3 mole %) was prepared and
evaluated in the same manner as above, good results in terms of **adhesive**
property and electrical conductance were attained similarly as in the cases of
using Ni and Mo.

US-PAT-NO: 6419849

DOCUMENT-IDENTIFIER: US 6419849 B1

TITLE: Method for manufacturing piezoelectric material

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Next, the lower electrode 30 is formed over the diaphragm film 20. For instance, a titanium film is formed in a thickness of 100 nm by sputtering over the diaphragm film 20 to obtain the lower electrode 30. When the lower electrode 30 is **platinum, an adhesive** layer of titanium, chromium, or the like (not shown) may be interposed between the diaphragm film 20 and the lower electrode 30 in order to increase the **adhesive** strength therebetween. This adhesive layer may be formed from titanium in a film thickness of 50 nm by sputtering.

US-PAT-NO: 6419848

DOCUMENT-IDENTIFIER: US 6419848 B1

TITLE: Piezoelectric actuator, ink-jet type recording head, manufacturing
method therefor, and ink-jet printer

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A bottom electrode 3 is formed following the formation of the diaphragm film 2.
The material of the bottom electrode 3 may be pure metal, an alloy, or an
electroconductive ceramic. Suitable examples include platinum, titanium,
palladium, rhodium, and other high-melting noble metals. Specifically, a film
with a thickness of 100 nm is formed by sputtering platinum to obtain a bottom
electrode 3. When the bottom electrode 3 is a platinum film, and adhesive
layer (not shown) composed of titanium, chromium, or the like may be interposed
in order to enhance the adhesion between the diaphragm film 2 and the bottom
electrode 3. This adhesive layer may, for example, be formed in a thickness of
50 nm by sputtering.

US-PAT-NO: 6277762

DOCUMENT-IDENTIFIER: US 6277762 B1

TITLE: Method for removing redeposited veils from etched platinum

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Referring in detail now to the drawings wherein similar parts of the present invention are identified by like reference numerals, there is seen in FIG. 1 a wafer, generally illustrated as 10, having a semiconductor substrate, generally illustrated as 12. The semiconductor substrate 12 includes regions of circuit elements which do not appear in the drawings, but are well known to those skilled in the art. A barrier layer 14 is disposed over the semiconductor substrate 12 and a platinum electrode layer 16 is disposed over the barrier layer 14. Because the platinum electrode layer 16 easily diffuses or reacts with certain elements (e.g. a poly-Si plug) within the semiconductor substrate 12, the barrier layer 14 is required between the platinum electrode layer 16 and the semiconductor substrate 12. The barrier layer 14 also functions as an adhesive for coupling the semiconductor substrate 12 to the platinum electrode layer 16. An insulation layer or mask 18 is disposed over the platinum electrode layer 16 and a resist 20 (i.e. a photoresist or photomask) is selectively positioned on the insulation layer 18 as best shown in FIG. 1. In another preferred embodiment of the invention as shown in FIG. 2, a protective layer 22 is disposed between the platinum electrode layer 16 and the insulation layer 18.

The barrier layer 14 may be any suitable barrier layer which is capable of dually functioning as an adhesive and a diffusion barrier to the platinum electrode layer 16. The barrier layer 14 may be of any suitable thickness. Preferably, the barrier layer 14 comprises titanium and/or a titanium alloy, such as TiN, and possesses a thickness ranging from about 50 Angstroms to about 600 Angstroms, more preferably from about 200 Angstroms to about 400 Angstroms, most preferably about 300 Angstroms. The barrier layer 14 is preferably disposed on the semiconductor substrate 12 by the RF magnetron sputtering method.